A Broadband InP Track-and-Hold Amplifier Using Emitter Capacitive/Resistive Degeneration

Shaojun Li, *Graduate Student Member, IEEE*, Yongbo Su, Hongliang Lv, *Member, IEEE*, Lei Zhou, Yimen Zhang, *Senior Member, IEEE*, Yuming Zhang, *Member, IEEE*, Jun Hu, Feng Yang, and Zhi Jin

***Abstract*— In this letter, we present a 24-GSa/s, >20-GHz wideband track-and-hold amplifier (THA) based on indium phosphide (InP) double-heterojunction bipolar transistor (DHBT) technology for high-speed sampling systems. In the proposed approach, the output pole of the input stage is canceled by the zero produced by the emitter capacitive/resistive degeneration, and the bandwidth is thereby extended without voltage drop. The compensation technique for V_{be} modulation in the output stage is introduced to reduce distortion. The monolithic microwave integrated circuit (MMIC) prototype occupies only 0.69 mm^2, and the experimental results show that it has a 0.112–f_T bandwidth from dc to 22.3 GHz, which is wider than any ratio reported compact THA solutions using the InP technology. In addition, a spurious-free dynamic range (SFDR) of better than 42 dB and total harmonic distortion (THD) of less than −25 dBc are demonstrated at a 24-GSa/s sampling rate. The THA consumes only 374 mW, which is among the lowest dc power dissipation reported for the InP technology.**

***Index Terms*— Analog-to-digital converter (ADC), double-heterojunction bipolar transistor (DHBT), indium phosphide (InP), monolithic microwave integrated circuit (MMIC), track-and-hold amplifier (THA).**

I. Introduction

THE track-and-hold amplifier (THA) has widely been used as a high-speed front-end circuit for an analog-to-digital converter (ADC). By using high-performance THA, the ADC's input analog bandwidth can be extended from megahertz to gigahertz. In addition, the overall performance of the receiver strongly depends on the ADC bandwidth, sampling rate, resolution, and linearity, so the THA must also have a wide input bandwidth, high sampling rate, and low harmonic distortion performance, making it plays an important role in applications such as wireless communications, software-defined radios, military radar systems, and instrumentation [1]. Recently, indium phosphide (InP) double-heterojunction bipolar transistor (DHBT) becomes an attractive technology for high-speed THAs with more than 10-GSa/s sampling rate [2] for its faster operation and good g_m–V_{BE} matching characteristics. These designs use either diode bridges or traditional switched emitter follower (SEF) as a sampling switch. Although wide bandwidth can be obtained in diode bridges, it is difficult to achieve a good linearity and a wide dynamic range due to the mismatching in current sources and pulse drivers [3]. The SEF topology has better linearity and dynamic range compared to the diode bridges and has been widely used for high-speed THAs that only n-p-n transistors are available. However, the potential instability may also appear in the traditional SEF stage when it drives a capacitive load [4].

This letter here reports a THA with a sampling rate of up to 24 GSa/s in 0.8-μm InP DHBT technology. The prototype uses the capacitive/resistive degeneration in the input stage to enhance bandwidth, and the small resistive degeneration is used in two SEF switches to improve linearity and stability. In conjunction with the well-designed clock buffer and clock lines layout, the THA is designed to achieve the target of 24-GSa/s sampling rate with over 20-GHz small-signal bandwidth in the track mode.

II. Technology

This 24-GSa/s high-speed THA chip has been realized with our in-house 0.8-μm InP DHBT technology [5]. The DHBT has a 40-nm-thick carbon-doped base layer, a 70-nm-thick undoped InP emitter, and a 250-nm-thick InGaAs composite collector. The transistor is grown on a 3-in Fe-doped InP wafer and the epitaxial profile is designed for high-frequency applications. When biased at a collector current of $I_C = 11.5$ mA and a collector-emitter voltage of $V_{CE} = 1.7$ V, the fabricated DHBTs with nominal 0.8×8 μm^2 emitter dimensions exhibits a current-gain cutoff frequency of $f_T = 199$ GHz. The DHBT technology used here has both base-emitter and base-collector heterojunctions that present a large energy barrier to holes, preventing significant hole injection from the base to the emitter or to the collector when they are forward biased. The hole minority carriers storage is thereby eliminated, and the storage time of minority carries becomes small. This is a key advantage of designing high-speed THA with the InP DHBT device. The technology features three metal Au interconnect layers and provides 50 Ω/sq. thin-film resistors, the 0.3 fF/μm^2 MIM capacitor is used as a hold capacitor (C_H) in this THA design.

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Shaojun Li was with the School of Microelectronics, Xidian University, Xi'an 710071, China. He is now with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China (e-mail: lishaojun@ime.ac.cn).

Yongbo Su, Lei Zhou, Jun Hu, Feng Yang, and Zhi Jin are with the Institute of Microelectronics, Chinese Academy Sciences, Beijing 100029, China (e-mail: jinzhi@ime.ac.cn).

Hongliang Lv, Yimen Zhang, and Yuming Zhang are with the School of Microelectronics, Xidian University, Xi'an 710071, China.

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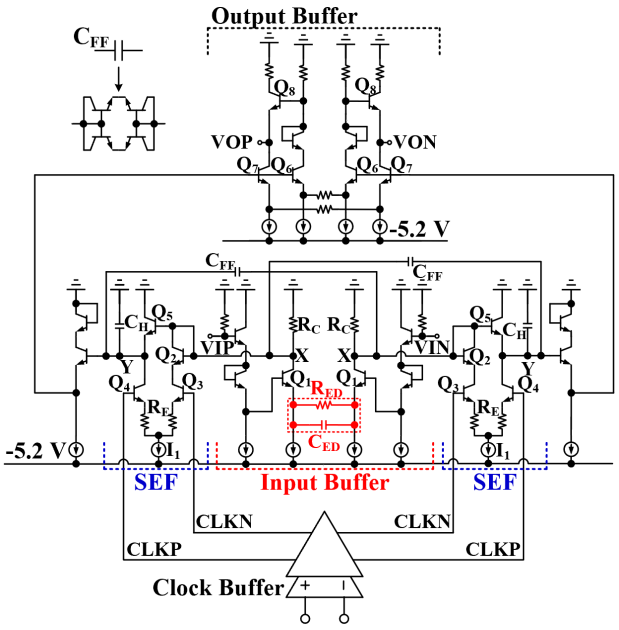


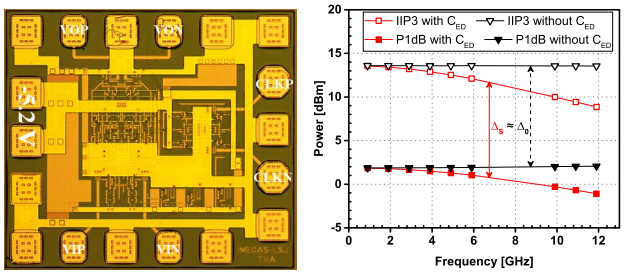
Fig. 1. Transistor-level schematic of the proposed THA.

III. Proposed Monolithic Microwave Integrated Circuit (MMIC) THA Design

The transistor-level schematic of the THA shown in Fig. 1 is fully differential and composed of capacitive/resistive degenerated emitter-coupled pair as the input stage, two resistive degradation SEF sampling switches with a feedthrough cancelation capacitor (C_{FF}), and a linear output buffer and a clock buffer which provides 24-GHz clock signals to the degeneration SEFs. The working principle of the THA can be summarized as a track-and-hold mode. In the track mode, clock signal CLKP is high, CLKN is low, and Q_4 steers the current source I_1 to flow through Q_5. Q_5 and current source I_1 act as a source follower to track the signal. In the hold mode, CLKP is low, CLKN is high, Q_3 steers the current I_1 to flow through R_C, Q_2, and $R_S E$. The base voltage of Q_5 then drops and it is turned off due to resistor R_C. As a result, the THA holds the data on the capacitor C_H, this provides greater timing margins in the ADC design. The input stage here is a bandwidth-enhanced amplifier to decouple the input signal source and hold capacitors. In addition, the high-speed THA uses a smaller hold capacitor to prevent bandwidth reduction, resulting in feedthrough of the input signal to the hold capacitor during the hold mode [6]. Therefore, two feedforward compensation capacitors (C_{FF}) are utilized to reduce this hold-mode feedthrough. Fig. 2(a) shows the die photograph of the proposed 24-GSa/s InP DHBT THA with an area of 780 μm $\times$ 880 μm.

A. Input Stage

The design of the broadband THA is mainly determined by the location of poles in its frequency response. The THA core circuit in Fig. 1(a) exhibits two main poles. The first pole is located at X, which is the output of the input stage. The second pole is at Y, which is formed by the hold capacitance and the effective resistance of the SEF switch with respect to ground. As mentioned earlier, there is a tradeoff between bandwidth and hold-mode distortion. To achieve low distortion in the first



(a) (b)

Fig. 2. (a) Die photograph of the 24-GSa/s THA. (b) Simulated IIP3 and P1dB of the input stage with and without C_{ED}.

Nyquist frequency range of 12 GHz, the minimum value of the hold capacitor estimated by the simulation should be larger than 180 fF, and the C_H of 200 fF is selected to guarantee the small-signal bandwidth to over 18 GHz while alleviating hold-mode distortion.

Once the hold capacitor is determined, the input stage becomes a more serious limitation for wider band THA design. For this reason, this work introduces a zero through capacitive/resistive degeneration (enclosed in the red dotted box) to create a broadband response. Considering the half-circuit of the input stage and its small-signal equivalent model, after a simple mathematical derivation, the expression of the circuit transconductance can be found by the following equation:

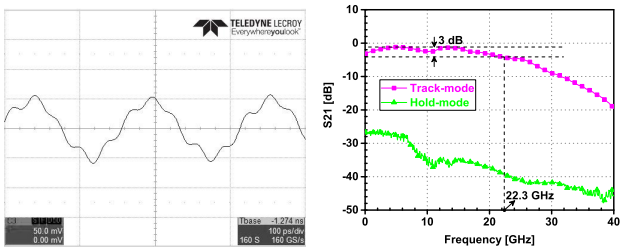
$$G_m = \frac{g_m(R_{\mathrm{ED}}C_{\mathrm{ED}}s + 1)}{\left(R_{\mathrm{ED}}C_{\mathrm{ED}}s + 1 + g_m\frac{R_{\mathrm{ED}}}{2}\right)} \tag{1}$$

then G_m contains a zero at $1/(R_{\mathrm{ED}}C_{\mathrm{ED}})$ and a pole at $(1+g_m R_{\mathrm{ED}}/2)/(R_{\mathrm{ED}}C_{\mathrm{ED}})$, where g_m is the transconductance of Q_1. If the zero cancels the pole at the output of the input stage, namely, if $R_{\mathrm{ED}}C_{\mathrm{ED}} = R_C C_X$, then the bandwidth of overall amplifier is extended to $(1 + g_m R_{\mathrm{ED}}/2)/(R_C C_X)$, it means that the speed is increased by a factor of $1+g_m R_{\mathrm{ED}}/2$ with the proposed capacitive/resistive degeneration. Here the capacitance C_X consists of the emitter-base capacitance C_{be} of the SEF switch and the junction capacitance C_{jo} of Q_1 at the output node X of the input stage. Taking into account the low frequency gain, circuit parameters are set to $R_C = 125\ \Omega$, $R_{\mathrm{ED}} = 120\ \Omega$, $C_{\mathrm{ED}} = 0.1$ pF, and the corresponding small-signal bandwidth is estimated to extend beyond 23 GHz.

However, the negative feedback of the emitter becomes weaker at high frequencies, resulting in the degeneration of linearity [7]. The simulated input third-order intercept (IIP3) and 1-dB compression point (P1dB) of the input stage in Fig. 2(b) also indicate that the bandwidth enhancement is obtained at the cost of linearity reduction. Nevertheless, the linearity figure of merit ($\Delta = \mathrm{IIP3} - \mathrm{P1dB}$) [8] remains the same above 10 dB, which shows that the bandwidth-linearity tradeoff of the proposed capacitive/resistive degeneration technique is acceptable depending on system requirements.

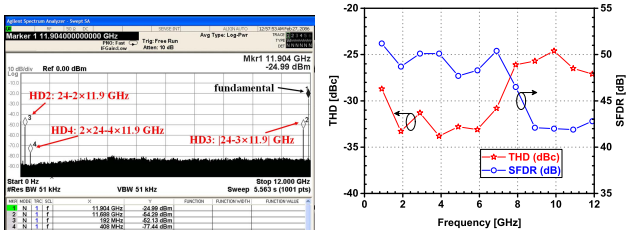
B. SEF Switches

The SEF is a key component of THA, and the differential SEF element can incorporate simple resistive degeneration to form negative feedback for improving stability and linearity [4]. Thus, the 15-Ω small resistors R_E are inserted into the emitters of switch pair Q_3 and Q_4 to prevent the



(a) (b)

Fig. 3. (a) Measured differential output waveform of a 6.1-GHz, −12-dBm input sinusoid signal. (b) Measured single-ended S-parameters.



(a) (b)

Fig. 4. (a) Measured single-ended spectrum of 11.9 GHz for THD at P1dB. (b) Measured single-ended THD and SFDR versus input frequencies.

significant consumption of voltage headroom. We also add the cross-coupled feedforward compensation capacitors ($C_{\rm FF}$) [9] to suppress the feedthrough due to the small hold capacitor mentioned before. Furthermore, since the input stage is still active in the hold mode, undesirable signals appear at the collector nodes of Q_1 and pass through the Q_5 base-emitter junction capacitance. At the same time, the $C_{\rm FF}$ transfers the unwanted signals with the same amplitude but opposite signs to offset the unwanted signals and reduce overall feedthrough.

C. Output Buffer and Clock Buffer

The output buffer is implemented as a highly linear emitter-degeneration amplifier proposed by Miki *et al.* [10], in which Q_7 generates the replica collector currents of Q_6 to bias Q_8, then counter modulation occurs at $V_{\rm be}$ of Q_8, which cancels the original $V_{\rm be}$ modulation of Q_6, high linearity is thereby achieved. A clock buffer consists of a two-stage open-loop amplifier is designed to have a differential signal with 300 mV per side swing, and each with a fan-out of two, the four differential outputs of the clock buffer drive two SEF switch pairs in-phase through double emitter-follower stages. In addition, small rising and falling time of clock signal with a bandwidth of exceeding 24 GHz are achieved using this clock buffer, so that the signal-to-noise ratio (SNR) and resolution are further improved.

IV. Measurement Results

The proposed alternative THA is measured via on-wafer with 150-μm spacing Infinity GSGSG dual probing arms. The Hyperlabs HL9405 wideband balun is used to implement the function of converting a differential signal to a single-ended output. In order to better characterize the transient performance of the THA, the bandwidth of subsequent instruments must be close to twice the sampling rate of this THA [11], a Lecroy WaveMaster 10-59Zi-A oscilloscope is thereby used to display the differential output waveform, the spectral content of the single-ended output signal is captured using an N9030A spectrum analyzer.

All of the measurement results reported at a sampling rate of 24 GSa/s. Fig. 3(a) illustrates that a 6.1-GHz, −12-dBm input signal is sampled by the proposed THA, and the measured differential time-domain waveform shows that the track-and-hold function is achieved, in which the balun used here has an amplitude and phase imbalance of ±0.1 dB and ±1°, respectively, [12]. The 22.3-GHz single-ended small-signal bandwidth of the THA in the track mode is also demonstrated in Fig. 3(b), which certifies the effectiveness of the bandwidth enhancement by capacitive/resistive degeneration, and the isolation in the hold mode is also better than 34 dB above 9 GHz.

TABLE I
Comparison With Other State-of-the-Art InP THAs

Ref.	[14]	[15]	[3]	[16]	**This work**
InP Process	DHBT	DHBT	DHBT	on-Si	**DHBT**
f_T (GHz)	210	320	370	300	**199**
BW (GHz)	15	16	27	25	**22.3**
BW/f_T	0.072	0.050	0.073	0.083	**0.112**
f_{sample} (GSa/s)	1	4	50	30	**24**
SFDR (dB)	-	44	55	60	**51.2**
THD (dBc)	-38.7	-38.6	-29.5	-59	**-27.1**
@F_{in} (GHz)	@15	@10	@15	@1	**@11.9**
P_{DC} (mW)	2100	2100	1200	420	**374**
Area (mm^2)	2.24	2.70	0.73	0.77	**0.69**

According to the definition of spurious-free dynamic range (SFDR) and total harmonic distortion (THD) in [13], the single-ended 11.9-GHz output spectrum at P1dB input power is shown in Fig. 4(a), the THD is −27.1 dBc under large-signal excitation. In this case, the measured SNR is 36.4 dB. It is expected that the second harmonic distortion (HD2) should be much lower when the circuit is measured and operated in differential mode. Fig. 4(b) shows the measured single-ended SFDRs of the harmonic power just exceeds noise floor and THDs at P1dB input power versus frequencies, the maximum SFDR of 51.2 dB appears at 0.9-GHz input frequency. The THA maintains the SFDR higher than 42 dB and the THD stays less than −25 dBc. Table I compares this work with other state-of-the-art similar bandwidth THAs. As highlighted, this letter offers a lower dc power dissipation, higher bandwidth ratio (BW/f_T), and compact solution compared to others.

V. Conclusion

In this letter, a broadband 24-GSa/s compact THA has been demonstrated in InP DHBT technology. The zero introduced by the capacitive/resistive degeneration cancels out the output pole in the input stage and the bandwidth is extended. The THA is validated experimentally and achieves excellent bandwidth-f_T ratio with only 374-mW dc power dissipation with a negative supply voltage of −5.2 V. The measurement results indicate an excellent performance and a great potential for providing high-speed THA modules used in the future advanced sampling systems.

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